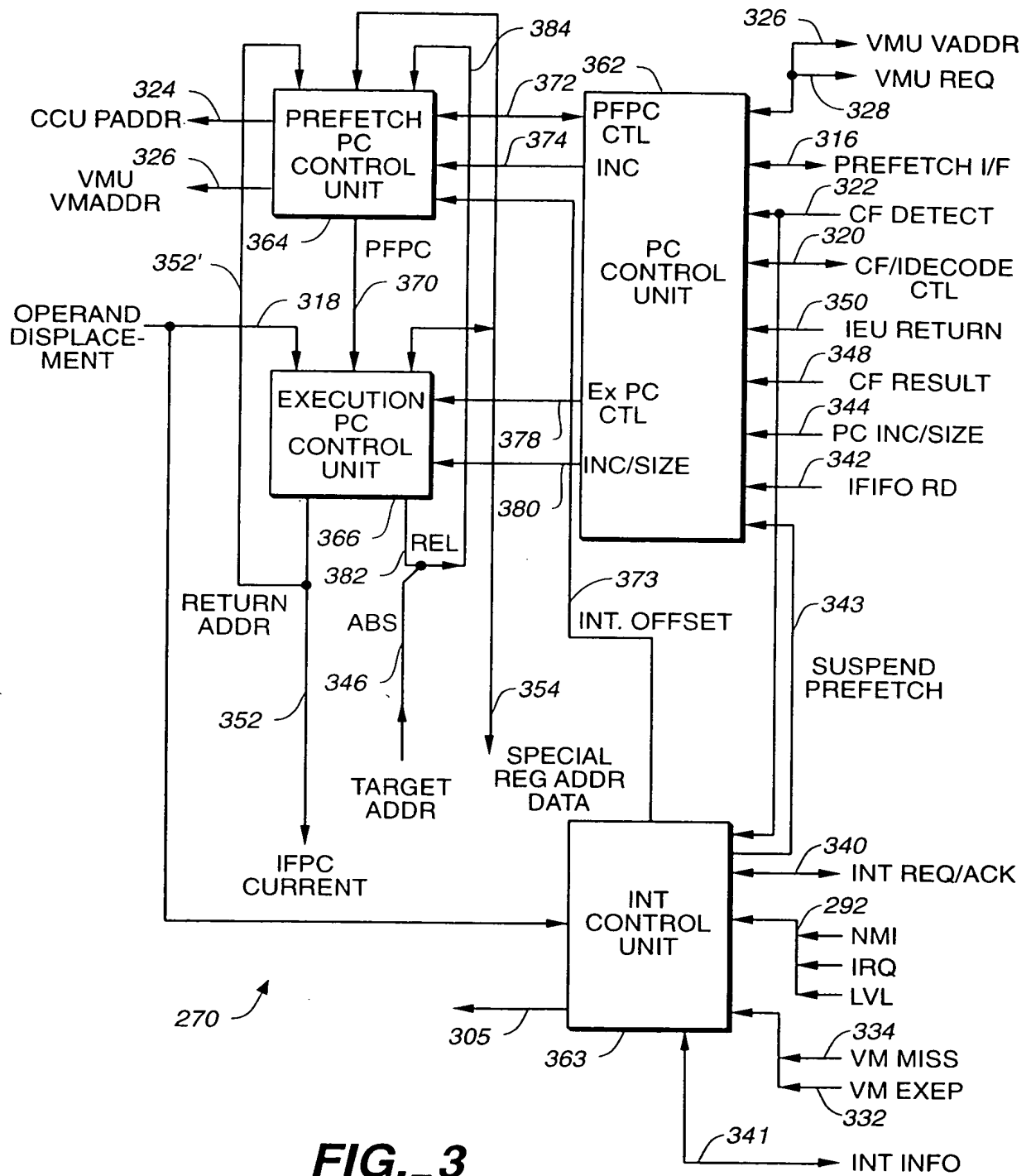
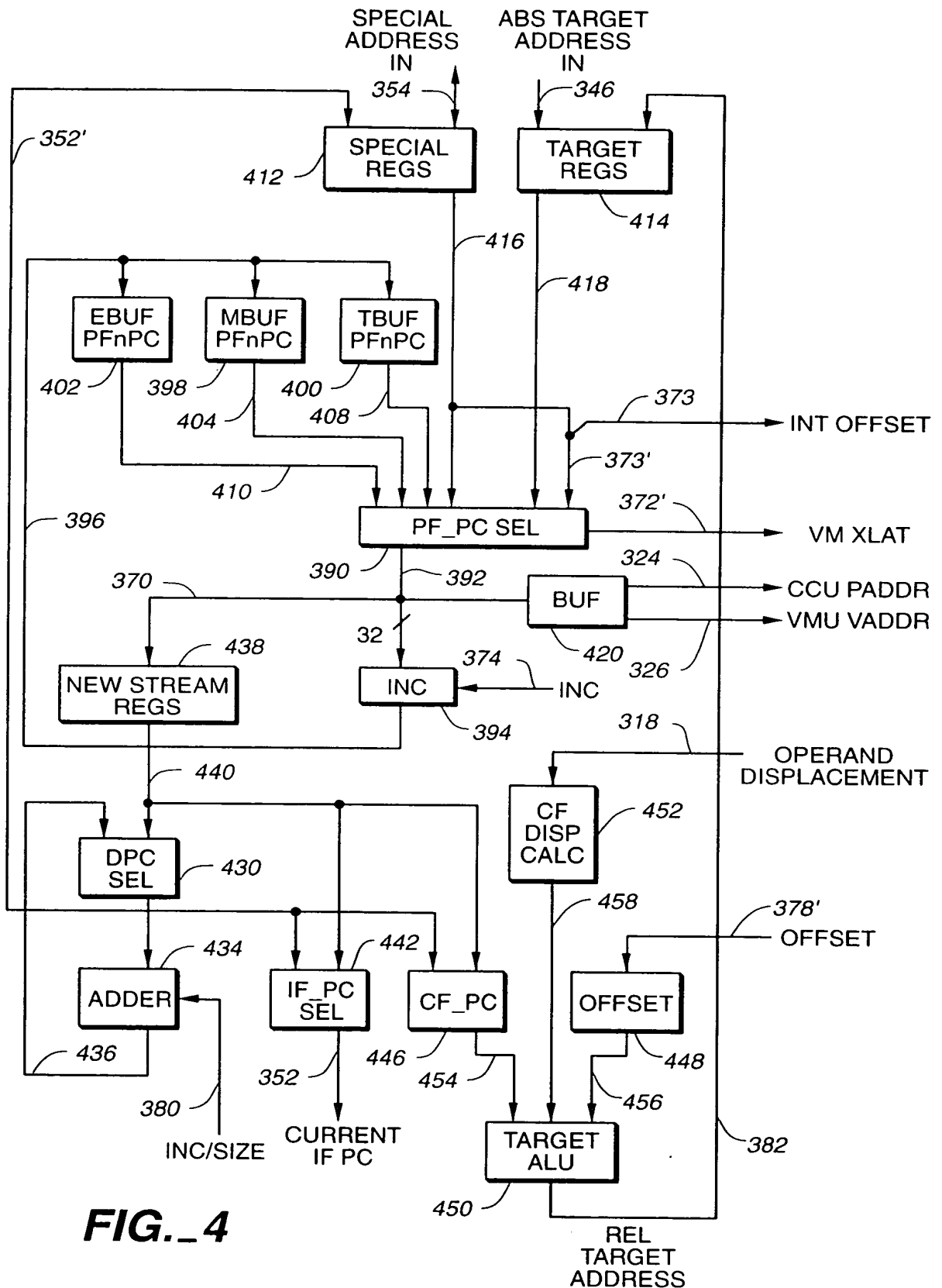


FIG. 1

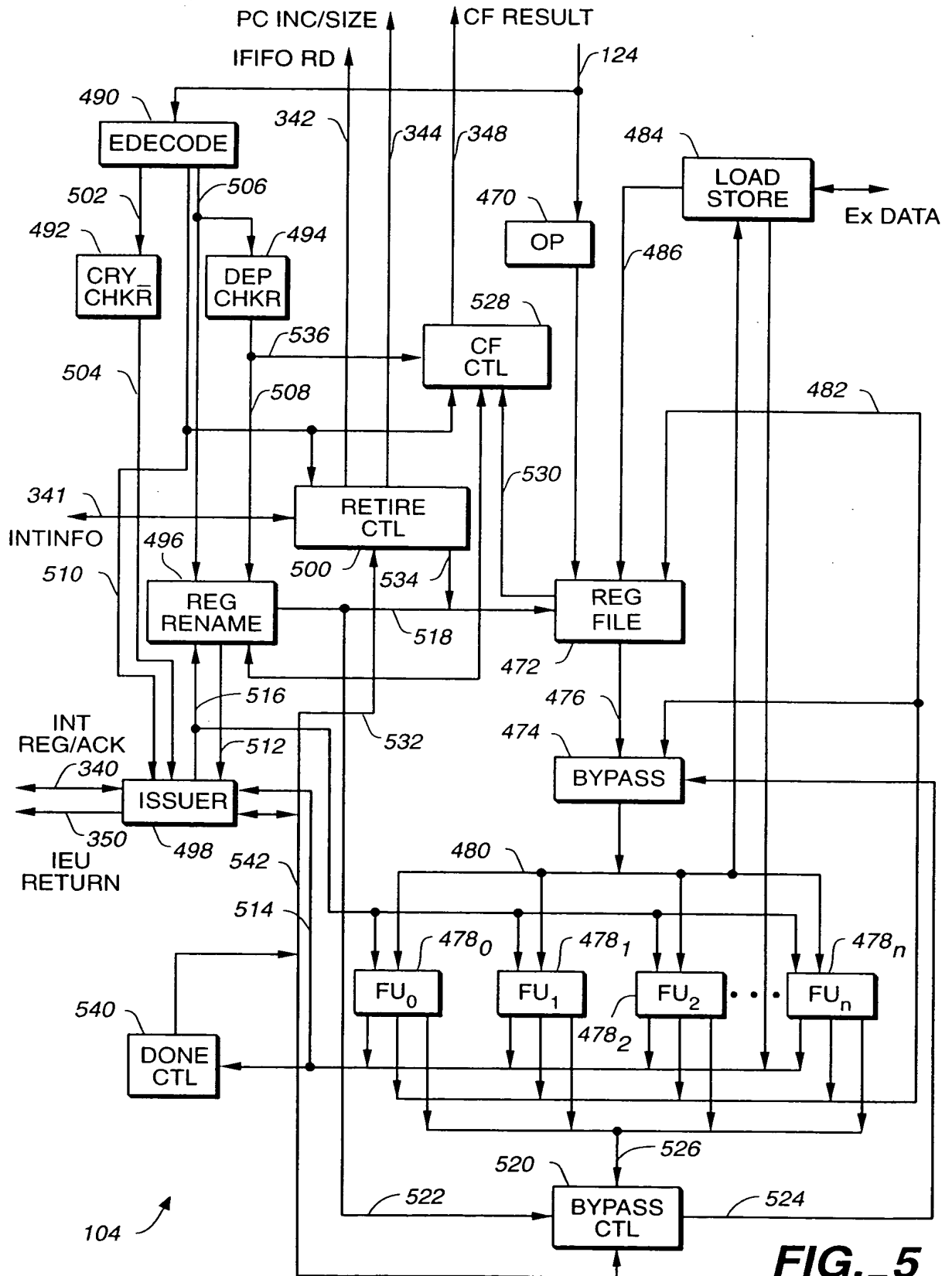




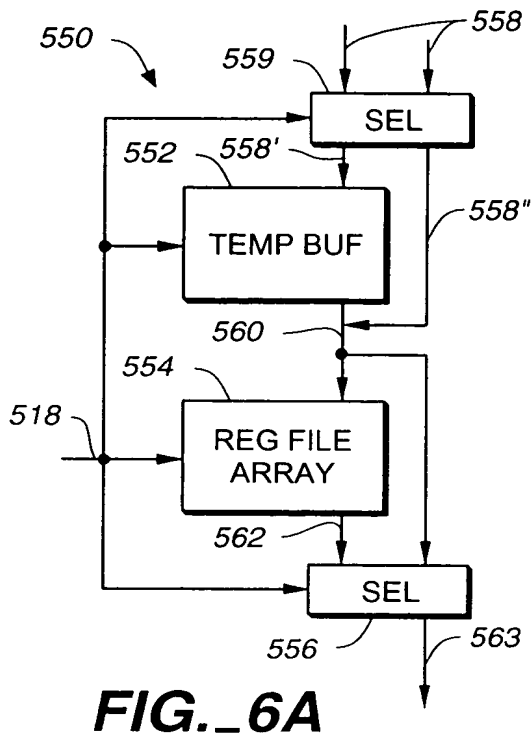
**FIG. 3**



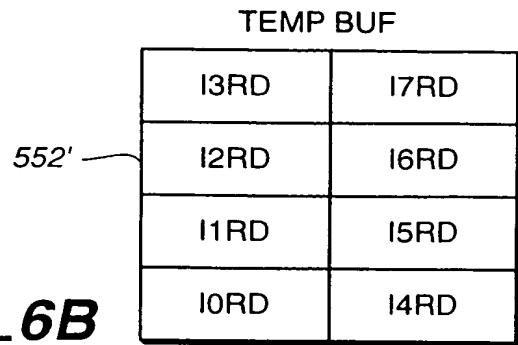
**FIG. 4**



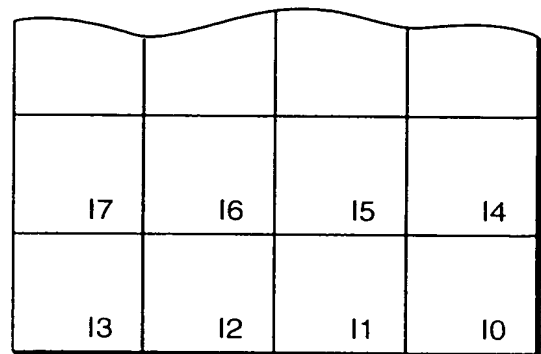
**FIG. 5**



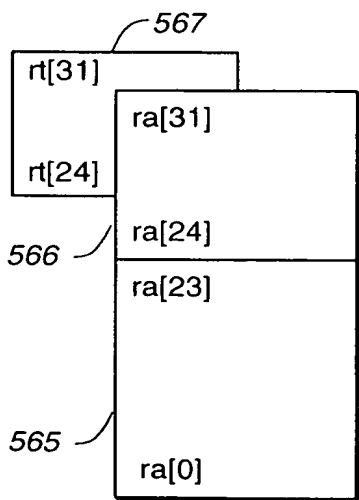
**FIG.\_6A**



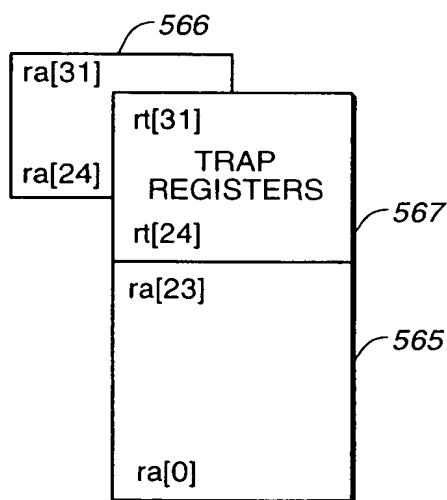
**FIG.\_6B**



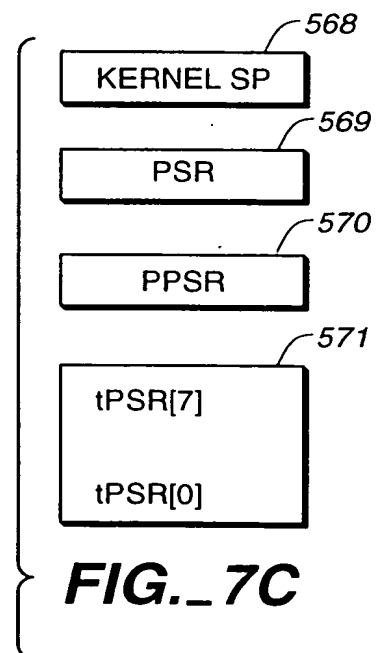
**FIG.\_6C**



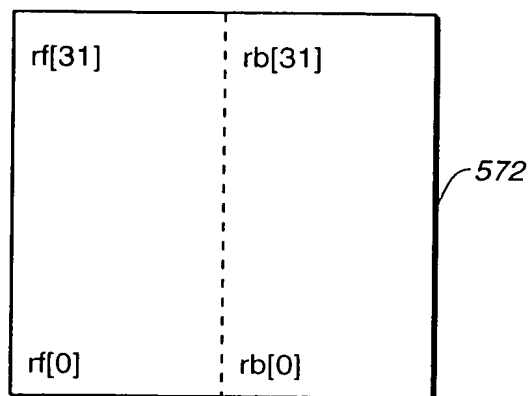
**FIG.\_7A**



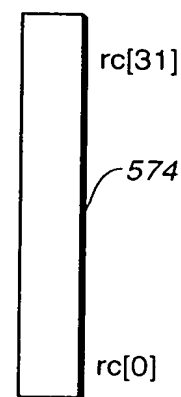
**FIG.\_7B**



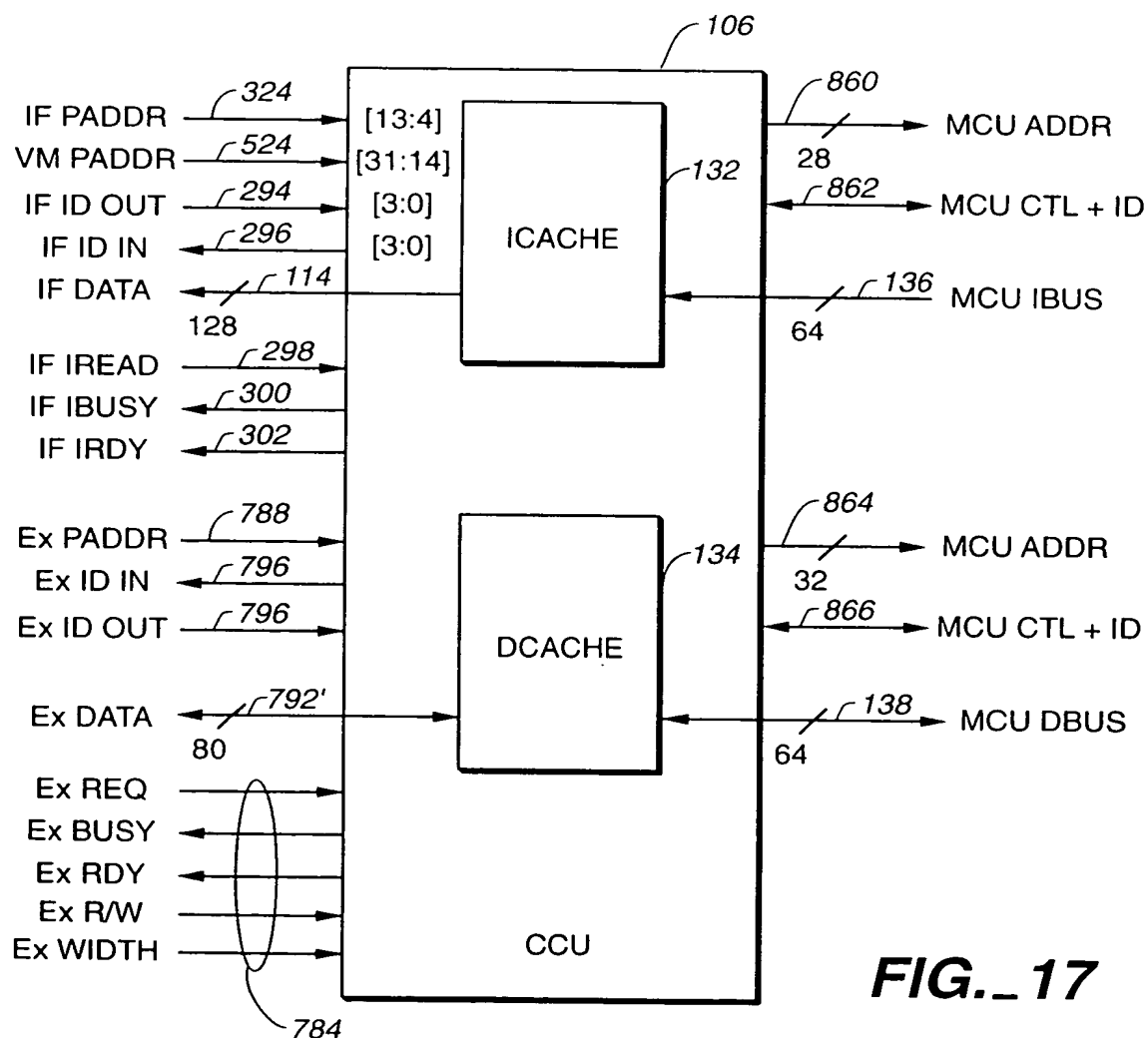
**FIG.\_7C**



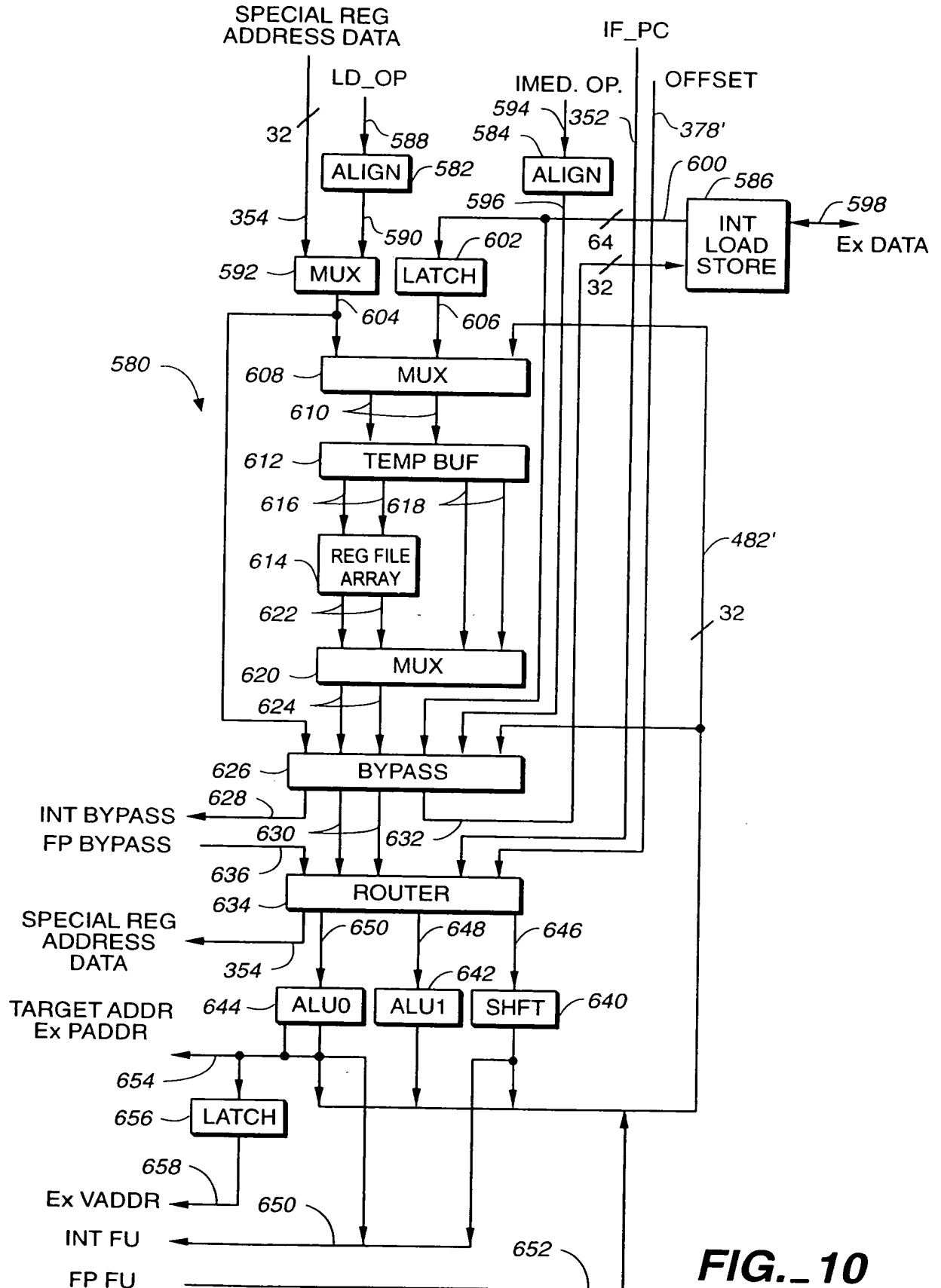
**FIG. 8**



**FIG. 9**

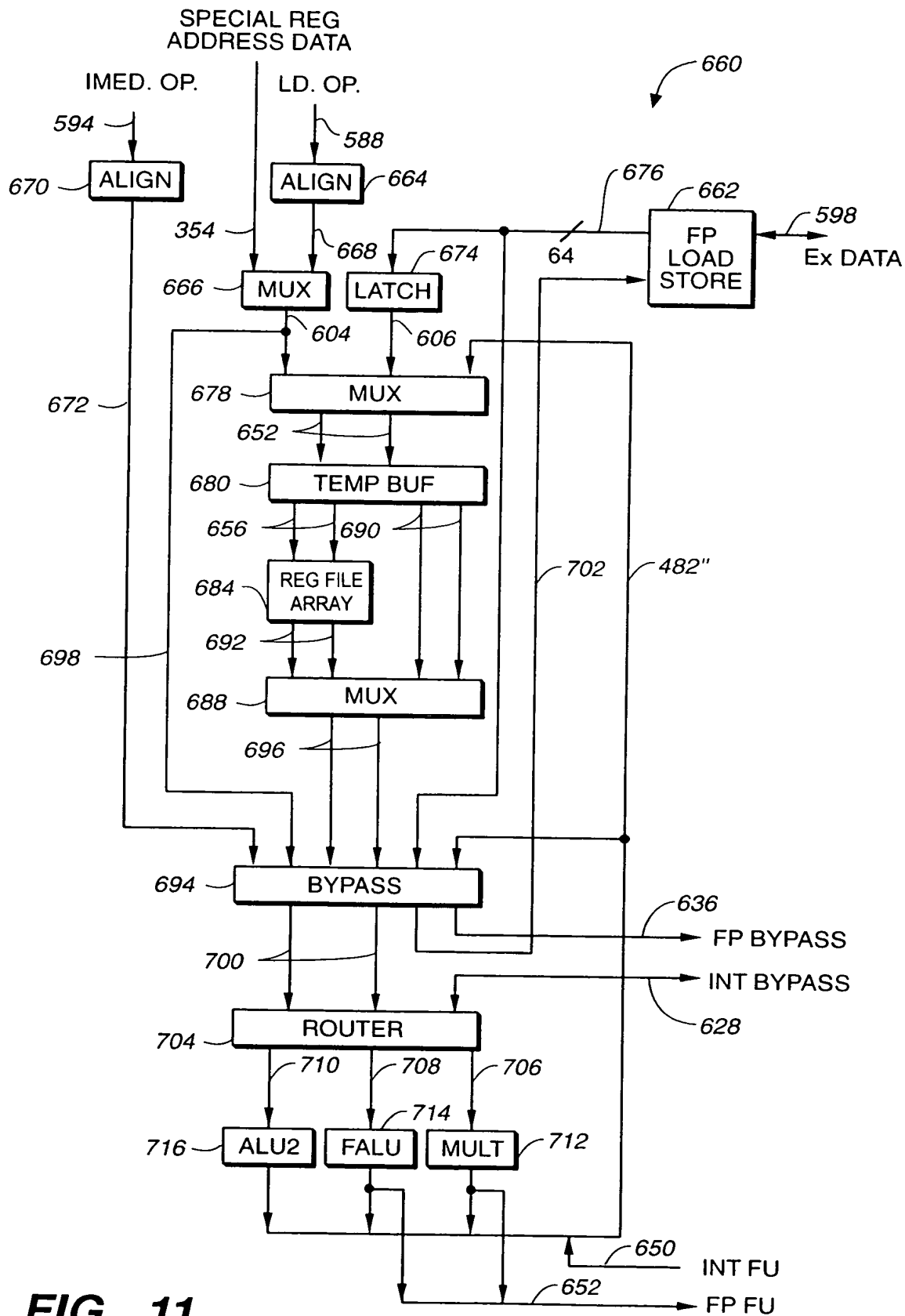


**FIG. 17**

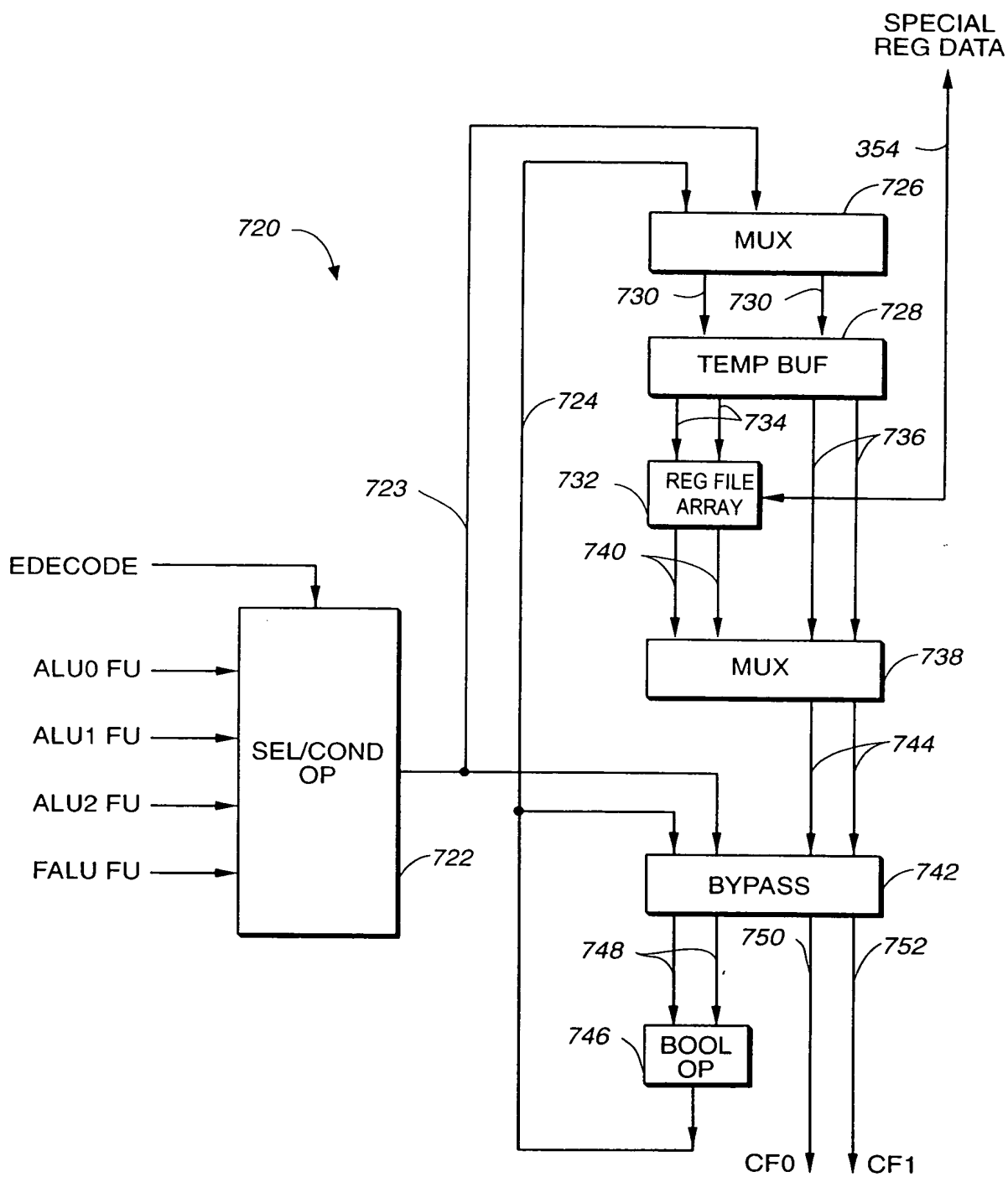


**FIG. 10**





**FIG. 11**



**FIG. 12**

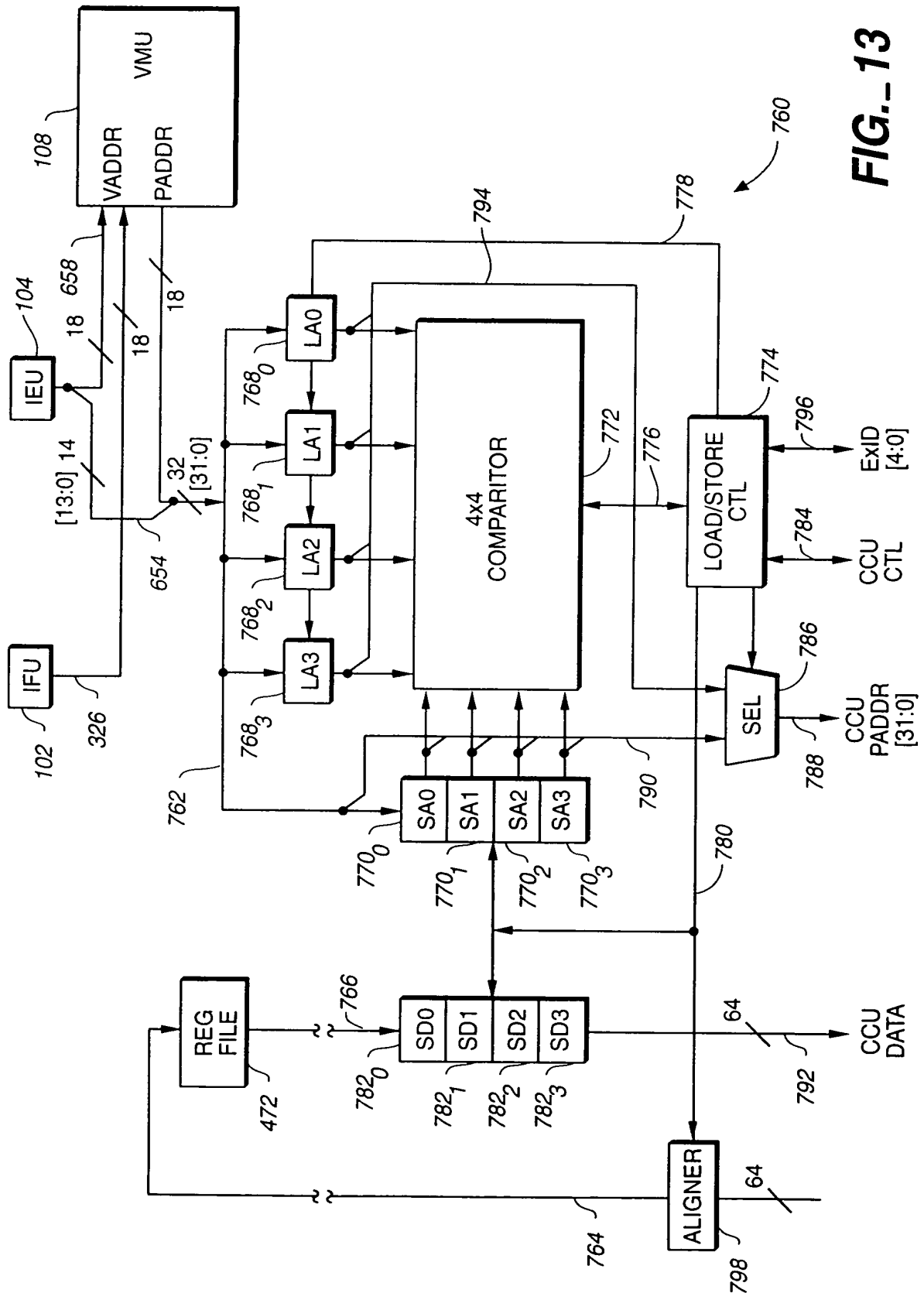


FIG. 13

Appl. No. *To Be Assigned*; Filed: HERewith  
 Dkt. No. SP015.C16; Group Art Unit: TBA  
 Inventor(s): NGUYEN et al.; Tel: 202/371-2600  
 Title: High-Performance, Superscalar-Based Computer System With  
 Out-Of-Order Instruction Execution

Replacement Sheet

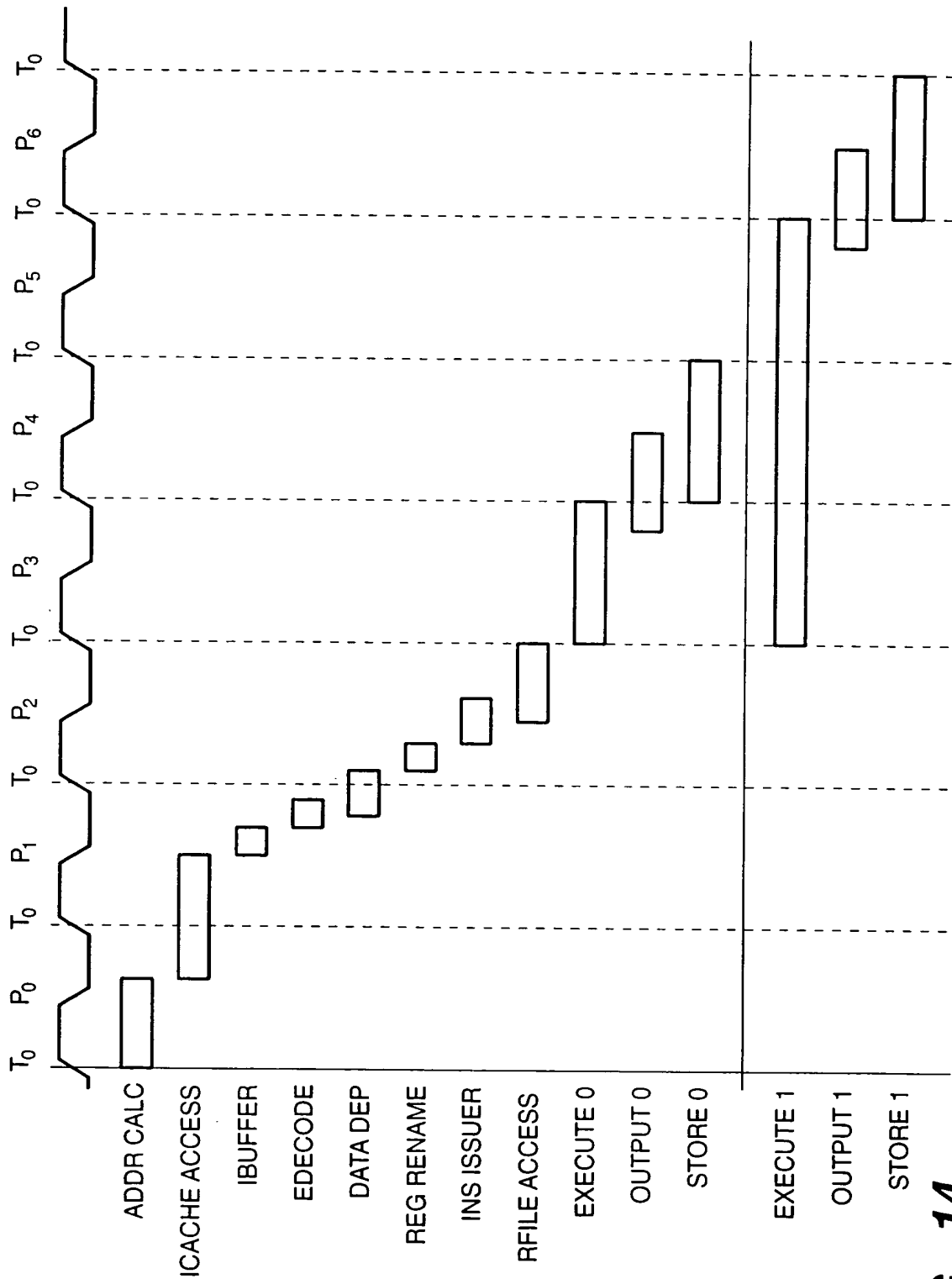


FIG. 14

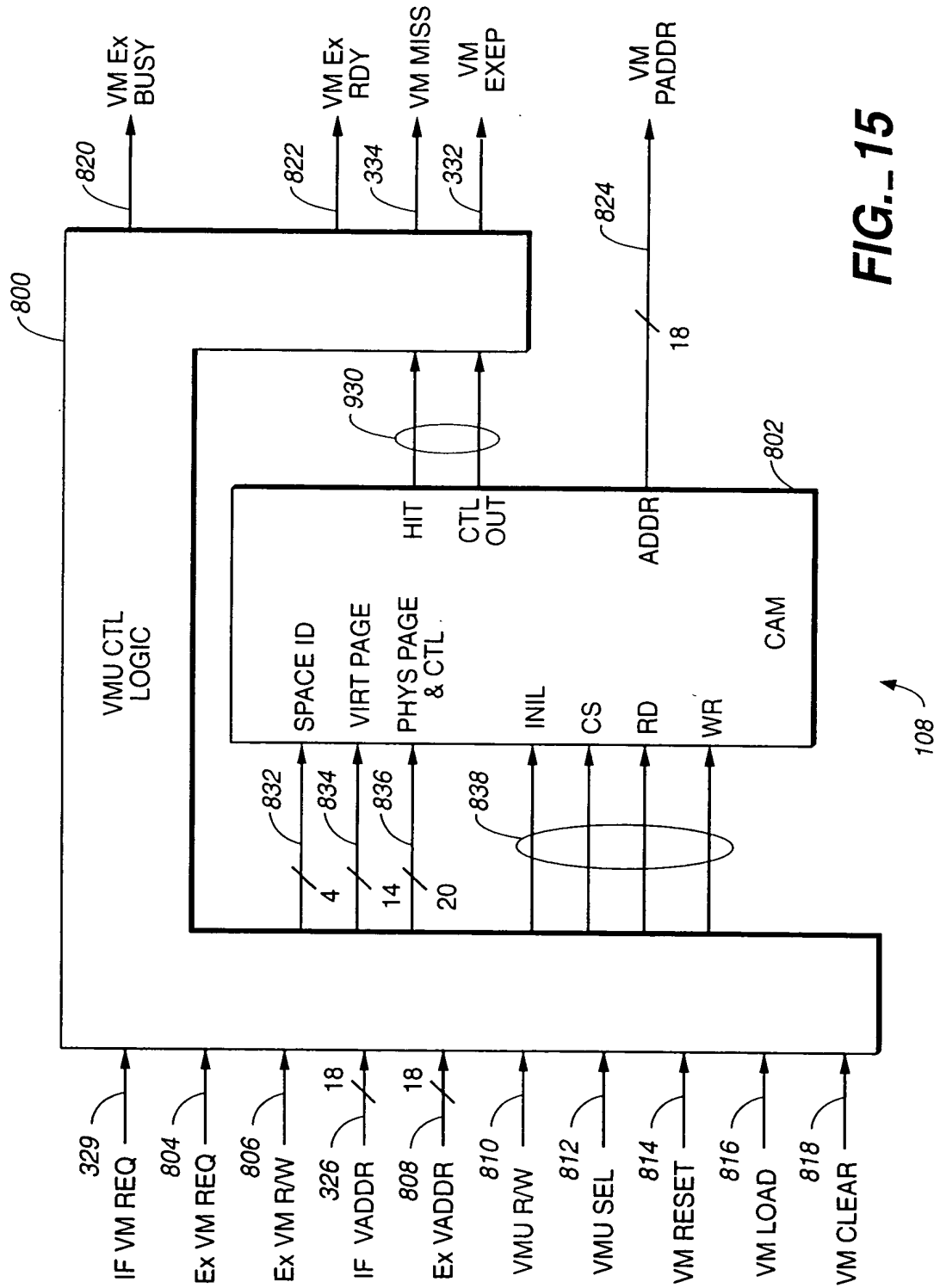
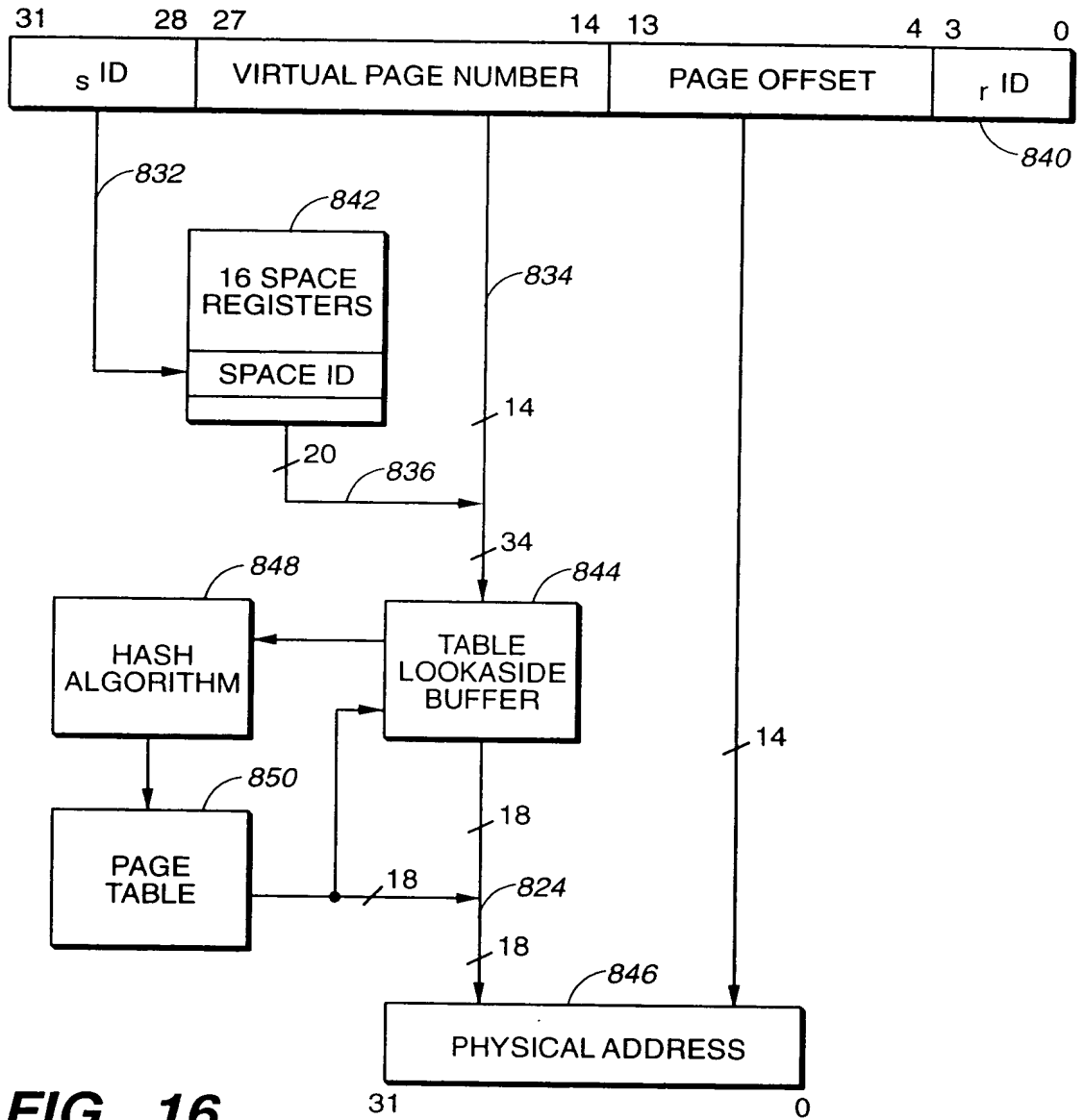


FIG. 15



**FIG. 16**